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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,277	08/28/2003	Yoshifumi Okabe	4041J-499DVE	8391

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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/651,277	OKABE ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 07/652,920.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/28/03, 10/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. Claims 24 and 27 are objected to because of the following informalities: Claim 24, line 2, the word "CZ" should be in full written form. Claim 27, line 2, the phrase "...form a surface.." is unclear whether it is being referred to "...from a surface...". Appropriate correction is required.

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 24-28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 58, 60, 61 and 64 of U.S. Patent No. 6,498,366 (Okabe et al.) in view of Sze.

In regards to claim 24, claim 58 of Okabe et al. disclose a semiconductor device. It comprising: a semiconductor substrate doped at an impurity concentration of between $7x10^{18}$ - $1x10^{21}$ cm^{-3}, said semiconductor substrate having a roughened rear surface a surface concentration of which is given by said impurity concentration (lines 2-7, 13-16); a semiconductor layer disposed over the semiconductor substrate (lines 4-5);

a power semiconductor element formed at a surface portion of the semiconductor layer (lines 8-9); a first metal layer forming a first electrode of said power semiconductor element, the first metal layer being located over said surface portion (lines 10-11); and a second metal layer forming a second electrode of said power semiconductor element, the second metal layer being located to contact said roughened rear surface of said semiconductor substrate (lines 12-19).

Okabe et al. differ from the claimed invention by not showing the semiconductor substrate is a CZ (Czochralski) semiconductor substrate.

Sze shows all silicon used for fabricating integrated circuits is prepared by the Czochralski technique.

Since both Okabe et al. and Sze disclose an integrated circuit formed on a silicon substrate, it would have been obvious to have the Czochralski silicon semiconductor substrate of Sze in Okabe et al. because it is a widely used semiconductor substrate.

In regards to claim 25, claim 58 of Okabe et al. show said semiconductor substrate is doped with arsenic at an arsenic concentration of between $7x10^{18}$ - $1x10^{21}$ cm^{-3}, said surface concentration of said roughened rear surface being given by said arsenic concentration (lines 2-4, 13-16).

In regards to claim 26, claim 60 of Okabe et al. further disclose said second metal layer comprises a metal selected from a group consisting of titanium (Ti), vanadium (V), chromium (Cr) and nickel (Ni).

In regards to claim 27, claim 61 of Okabe et al. further disclose a thickness from a surface of said first metal layer to said roughened rear surface of said semiconductor substrate is 200 - 450 microns.

In regards to claim 28, claim 64 of Okabe et al. further disclose said roughened rear surface of said semiconductor substrate has a surface roughness of between 0.2 - 0.6 microns.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
September 19, 2004

Steven Loke
Primary Examiner